



(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131315

Roll No.

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## B. Tech.

(SEM. III) (ODD SEM.) THEORY  
EXAMINATION, 2014-15

### SWITCHING THEORY AND LOGIC DESIGN

Time : 2 Hours]

[Total Marks : 50

- Notes :**
- (1) Attempt all questions.
  - (2) All question carry equal marks.

1. Attempt any four parts of the following :  $3.5 \times 4 = 14$
- (a) Convert the following numbers into desired base :
    - (i)  $(A6BF5)_{16} = (?)_2 = (?)_{\text{Gray}}$
    - (ii)  $(17 - 135)$  using 2's complement
  - (b) Simplify the following Boolean expression to a minimum number of literals :
    - (i)  $\overline{A}\overline{C} + ABC + A\overline{C} + A\overline{B}$
    - (ii)  $(\overline{x}\overline{y} + z) + z + xy + wz$
  - (c) Simplify the following expression into Product of sum(POS) form
    - (i)  $ABC\overline{D} + A\overline{B}D + BCD$
    - (ii)  $AC\overline{D} + \overline{C}D + A\overline{B} + ABCD$

- (d) Use Quine-Mc-Clusky (QM) method to solve the following function :

$$F(A,B,C,D) = \Sigma(5,7,8,9,10,11,14,15)$$

- (e) Simplify the Boolean function 'Y' together with don't care condition 'd' using k-map and implement it with two level NAND gate circuit.

$$Y = BD + BCD + ABCD$$

- (f) For the Hamming code 1001101001 received at the receiver end, correct this code for error if any ?



2. Attempt any two parts of the following :  $6 \times 2 = 12$

- (a) Design a BCD to 7 segment decoder. Assume positive logic, minimize the function.

- (b) Design the following Boolean function using  $4 \times 1$  Multiplexer.

$$F(A,B,C,D) = \Sigma m(0, 1, 3, 4, 8, 9, 15)$$

- (c) Design and explain the logic and circuit of 4 bit magnitude comparator.

3. Attempt any two parts of the following :  $6 \times 2 = 12$

- (a) Distinguish between synchronous and asynchronous digital sequential circuit. Design Module-5 Counter.

- (b) Explain race around condition and its remedy in brief. Realise T flip flop to SR flip flop.

- (c) Write down the classification of semiconductor memories. Draw and explain the programmable logic array (PLA).

4. Attempt any two parts of the following :  $6 \times 2 = 12$

- (a) Explain hazard and its types. Define critical race and non critical race. Also explain the elimination of hazards in asynchronous circuits.

- (b) With the help of diagram, explain the operations of Universal shift register.

- (c) An asynchronous sequential circuit described by the following excitation and output functions.

$$Y = X_1 X_2 + (X_1 + X_2)y \text{ and } z = y.$$

Where  $X_1$  and  $X_2$  = Input variables

Y = Excitation function

Z = Output function.

- (i) Draw the logic diagram of the circuit.

- (ii) Derive transition table.

- (iii) Output map and obtain a flow table.

