(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0109 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. III) THEORY EXAMINATION, 2012-13

DIGITAL LOGIC DESIGN

Time : 3 Hours] ***[Total Marks : 100***

SECTION – A

1. Attempt **all** parts : **10 × 2 = 20**

(a) Find 9's and 10's complement of the following decimal numbers :

(i) 24,681,234

(ii) 63,325,600

(b) Convert each of the following expressions into sum of products and products of sums :

(AB + C) (B + C 'D) X' + X (X + Y') (Y + Z')

(c) Convert the following to the other canonical form.

$F(x, y, z) = \sum (2, 4, 6, 7)$

(d) Implement the following expression using NOR gates

$F(w, x, y, z) = w'x' + x'z'$

(e) Construct 4 input priority encoder using combinational gates.

(f) Differentiate Ring Counter and Johnson Counter.

(g) Generate square wave output using D flip-flop.

(h) The contents of a four-bit register are initially 1001. The register is shifted six times to the right, with the serial input being 1010011. What are the contents of the register after two shifts ?

(i) How many address lines and input-output data lines are needed in 64K × 8 memory unit ?

(j) Define Primitive Flow Table.

SECTION – B

2. Attempt any **three** parts : **10 × 3 = 30**

(a) (i) Draw a NAND logic diagram that implements the complement of the following function :

$$F(A, B, C, D) = \Sigma(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$$

(ii) Simplify the following Boolean function, using Karnaugh maps.

$$F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 10, 13)$$

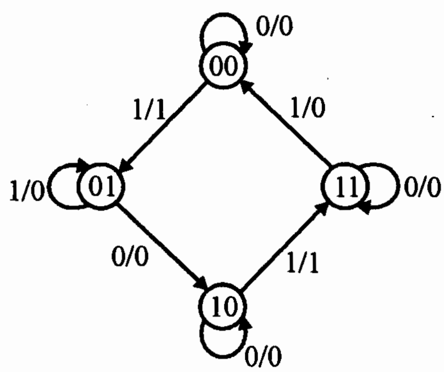
(b) (i) Design a 4-bit magnitude comparator using combinational gates.

(ii) Design a 4-bit Priority Encoder.

(c) Simplify the logic function given below, using Quine McClusky minimization technique and Realize simplified expression using universal gates.

$$F(A, B, C, D) = \Sigma\, m(0, 1, 3, 7, 8, 9, 11, 15)$$

(d) Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D flip-flop.



(e) Describe the general procedures that must be followed to ensure a race-free state assignment with example.

SECTION – C

Attempt **all** parts. **10 × 5 = 50**

3. Attempt any **two** parts :

(a) Show that a positive logic NAND gate is a negative logic NOR gate and vice versa.

(b) Simplify the Boolean function $F(A, B, C, D) = \Sigma(1, 3, 7, 11, 12, 13)$ which has the don't care condition $d(A, B, C, D) = \Sigma(0, 2, 5, 9)$ and then express the simplified function in sum-of-minterms form.

(c) Explain VEM Reading Principle with example.

4. Attempt any **one** part.

(a) Design a 4-bit universal shift register using positive edge triggered D flip-flops to operate as shown in table below :

Select line S_0	Select line S_1	Data line selected	Register operation
0	0	I_0	HOLD
0	1	I_1	Shift RIGHT
1	0	I_2	Shift LEFT
1	1	I_3	Parallel load

(b) Distinguish between Moore and Mealy model with necessary block diagrams.

5. Attempt any **two** parts :

(a) Design a 4 × 16 Decoder using 3 × 8 decoders.

(b) Implement a full subtractor with a decoder and NAND gates.

(c) Show that the characteristic equation for the complement output of JK flip-flop is $Q'(t+1) = J'Q' + KQ$

6. Attempt any **one** part.

(a) Design and explain the working of Binary multiplier.

$$C(x, y, z) = \Sigma(2, 5, 6, 7)$$

(b) Design a Four bit binary counter with parallel load.

7. Attempt any **two** parts.

(a) Explain Address multiplexing block diagram for a 64K DRAM.

(b) Design a data path for expression A = A + 3 and A = A + B.

(c) Explain Flow Table and Race Conditions in asynchronous sequential circuit design.