(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0110 Roll No. | | | | | | | | | | |

B.Tech.

(SEMESTER-IV) THEORY EXAMINATION, 2011-12

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note : Attempt **all** Section as directed.

Section – A

1. Attempt **all** questions from this section. **10 × 2 = 20**

   (a) Explain Von Neumann architecture.

   (b) What is bus arbitration ? List different types of bus arbitration.

   (c) Explain the concept of stack organization. Let SP = 00000 in the stack. How many items are there in the stack of FULL = 1 and EMPTY = 0 ?

   (d) Explain Hamming code with example.

   (e) What is the difference between a microprocessor and a microprogram ? Is it possible to design a microprocessor without a microprogram ?

   (f) What is the difference between a direct and an indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor register ?

   (g) Explain Address space and Memory space.

   (h) What is cache memory ? Why it is implemented ?

   (i) Why I/O devices cannot be connected directly to the system bus ?

   (j) What do you mean by vector interrupt ? Explain.

Section – B

2. Attempt any **three** parts from the following : **3 × 10 = 30**

   (a) Explain IEEE standard for floating point representation. Represent – 791.1258_{10} in IEEE double precision format.

(b) Write a program to evaluate the arithmetic statement

$X = (A - B + C * (D * E - F))/(G + H * K)$

(i) Using a general register computer with three address instructions.

(ii) Using an accumulator type computer with one address instructions.

(iii) Using a stack organized computer with zero-address operation instructions.

(c) Explain the subcycles of instruction cycle with example.

(d) A computer uses RAM chips of 1024 × 1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes ?

(e) Draw and explain the block diagram of typical DMA controller.

Section – C

Attempt **all** the questions : **5 × 10 = 50**

3. Explain the concept of bus and memory transfer. Explain the implementation of common bus using multiplexers.

OR

Explain carry lookahead adder. Assume each gate level delay = 0.001 μS. What will be the delay at carry lookahead 4-bit adder ?

4. A general register organization has 16 register with 32 bits in each ALU and a destination decoder.

(a) How many multiplexers are there in the A bus and what is the size of each multiplexer ?

(b) How many selection inputs are needed for MUX A and MUX B ?

(c) How many inputs and outputs are there in the decoder ?

(d) Formulate a control word for the system assuming that the ALU has 35 operations.

OR

Explain the hardware for implementation of Booth multiplication. Find which is the worst case for implementing Booth's algorithm for multiplication.

(a) 01110000

(b) 00000111

(c) 101010101

5. Draw and explain hardwired control unit. Compare hardwired control unit and microprogrammed control unit.

OR

Explain microprogram sequencer with block diagram. Compare horizontal and vertical organisation.

6. Explain various cache mapping techniques. A computer system has a 4K word cache organized in block set associative manner with 4 blocks per set, 64 words per block. The main memory contain 65536 blocks. How many bits are there in each of the TAG, SET and WORD fields ?

OR

What is virtual memory ? A virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block sizes of 1 K words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is (a) FIFO, (b) LRU.

7. What is an interrupt ? Explain how processor responds to an interrupt.

OR

Write short notes on :

(a) Programmed I/O

(b) Interrupt driven I/O

(c) DMA controlled I/O