## B. Tech.

## (SEM. IV) THEORY EXAMINATION 2011-12

## COMPUTER ORGANIZATION

*Time : 3 Hours*

*Total Marks : 100*

**Note :—** (1)  Attempt *all* questions.

(2)  All questions carry equal marks.

1.   Attempt any *four* parts of the following :—

(a)  What is overflow ? Discuss the differences among positive overflow, exponent overflow and significand overflow.

(b)  Represent the following decimal numbers in IEEE standard floating point format :—

(i)   – 1.75

(ii)  21

(c)  Discuss the generations of computer system.

(d)  What is memory transfer ? What are different registers associated for  memory transfer ? Discuss.

(e)  What is the benefit of using a multiple bus architecture compared to a single bus architecture ?

(f)  Discuss the bus arbitration.

(a) Explain the Booth's multiplication method and use this method to multiply decimal numbers – 23 and 9. Discuss the advantages of using this method.

(b) Write short notes on the following :—

    (i) direct addressing

    (ii) displacement addressing.

(c) Discuss the advantages and disadvantages of using a variable length instruction format.

(d) What is CISC ? Explain its characteristics.

(e) What is the stack organization ? Compare register stack and memory stack.

(f) Assuming that all registers initially contain O, what is the value of $R_1$ after the following instruction sequence is executed :—

    MOV  $R_1$, # 6

    MOV  $R_2$, # 5

    ADD  $R_3$, $R_1$, $R_1$

    SUB  $R_1$, $R_3$, $R_2$

    MULT $R_3$, $R_1$, $R_1$.

3. Attempt any *two* parts of the following :—

(a) Explain what is meant by a hardwired implementation of a control unit.

(b) Explain the different cycles of an instruction execution.

    (i) Micro operation

    (ii) Micro instruction

    (iii) Micro program

    (iv) Micro code.

4. Attempt any *two* parts of the following :—

(a) Explain the function of arithmetic circuit with the help of circuit diagram.

(b) Why is memory system of a computer organized as a hierarchy ? Discuss the basic elements of a memory hierarchy.

(c) What is meant by cache mapping ? What are different types of mapping ? Discuss different mapping techniques with examples.

5. Attempt any *two* parts :—

(a) Define interrupt. When a device interrupt occurs how does the processor determine which device has issued the interrupt ?

(b) When a DMA module takes control of a bus and while it retains control of the bus, what does the processor do ?

(c) List and define three techniques for performing I/O job.